REMARKS

This Preliminary Amendment is filed in order to facilitate processing the above identified application and responds to the Office Action dated November 24, 2008 in which the Examiner rejected claims 1-3, 7, 11-13 and 17 under 35 U.S.C. § 102 (e) and rejected claims 4-6, 8-10, 14-16 and 18-20 under 35 U.S.C. § 103.

Attached to this Amendment is a replacement sheet for Figure 11 to replace the Japanese script with English. Support for this change can be found within the Specification and within Figure 17. Applicant respectfully requests the Examiner approves the correction.

As indicated above, claims 1, 2, 8, 10-12, 18 and 20 have been amended in order to make explicit what is implicit in the claims. The amendment is unrelated to a statutory requirement for patentability.

Claims 1-2, 8 and 10 claim a multiplexing apparatus and claims 11-12, 18 and 20 claim a multiplexing method. The multiplexing apparatus and method calculate an order of multiplexing data units based on storage location and generate a plurality of multiplexing instruction data which describe the storage location and order of multiplexing of each data unit. A multiplex stream is generated by reading the multiplexing instruction data sequentially from the memory.

By (a) calculating an order of multiplexing based on storage location and (b) generating a plurality of multiplexing instruction data which describe (both) the storage location and order of multiplexing as claimed in claims 1-2, 8, 10-12, 18 and 20, the claimed invention provides a multiplexing apparatus and method which reduces the processing burden on a CPU since the CPU does not have to transfer an instruction directly to a multiplexor at the time of transfer but instead the multiplex stream is generated by reading the multiplexing instruction data. The prior art does not show, teach or suggest the invention as claimed in claims 1-2, 8, 10-12, 18 and 20.

Claims 1-3, 7, 11-13 and 17 were rejected under 35 U.S.C. § 102 (e) as being anticipated by *Robinett, et al.* (U.S. Publication No. 2002/0126711).

Robinett, et al. appears to disclose a DMA control circuit 116 which obtains control of a sufficient number of descriptor storage locations, and the packet storage locations to which they point, in the cache 114. The DMA control circuit 116 obtains control of such descriptor and transport packet storage locations for the cache 114. This enables continuous allocation of the descriptors and transport package storage locations to incoming transport packets as they are needed [0076].

Thus, *Robinett, et al.* merely discloses a control circuit 116 which obtains control of descriptor and transport packet storage locations. Nothing in *Robinett, et al.* shows, teaches or suggests (a) calculating an order of multiplexing data units based on storage location and (b) generating a plurality of multiplexing instruction data which describe (both) the storage location and order of multiplexing of each data unit as claimed in claims 1-2 and 11-12. Rather, *Robinett, et al.* only discloses a control circuit obtaining control of descriptor and transport packet storage locations.

Since nothing in *Robinett, et al.* shows, teaches or suggests (a) calculating an order of multiplexing data units based on storage location and (b) generating a plurality of multiplexing instruction data which describe the storage location and order of multiplexing as claimed in claims 1-2 and 11-12, Applicant respectfully requests the Examiner withdraws the rejection to claims 1-2 and 11-12 under 35 U.S.C. § 102 (e).

Claims 3, 7, 13 and 17 recite additional features. Applicant respectfully submits that claims 3, 7, 13 and 17 would not have been anticipated by *Robinett, et al.* within the meaning of 35 U.S.C. § 102 (e) at least for the reasons as set forth above. Therefore, Applicant respectfully

requests the Examiner withdraws the rejection to claims 3, 7, 13 and 17 under 35 U.S.C. § 102 (e).

Claims 4-6 and 14-16 were rejected under 35 U.S.C. § 103 as being unpatentable over *Robinett, et al.* in view of *Kelly, et al.* (U.S. Publication No. 2001/0036355).

Applicant respectfully traverses the Examiner's rejection of the claims under 35 U.S.C. § 103. The claims have been reviewed in light of the Office Action, and for reasons which will be set forth below, Applicant respectfully requests the Examiner withdraws the rejection to the claims and allows the claims to issue.

As discussed above, since nothing in *Robinett, et al.* shows, teaches or suggests the primary features as claimed in claims 1-2 and 11-12, Applicant respectfully submits that the combination of the primary reference with the secondary reference to *Kelly, et al.* would not overcome the deficiencies of the primary reference. Therefore, Applicant respectfully requests the Examiner withdraws the rejection to claims 4-6 and 14-16 under 35 U.S.C. § 103.

Claims 8-9 and 18-19 were rejected under 35 U.S.C. § 103 as being unpatentable over *Robinett, et al.* in view of *Dobson, et al.* (U.S. Patent No. 6,188,703).

As discussed above, *Robinett, et al.* only discloses a control circuit 116 which obtains control of descriptor and transport package storage locations. Nothing in *Robinett, et al.* shows, teaches or suggests (a) calculating an order of multiplexing data units based on storage location and generating a plurality of multiplexing instruction data which describe the storage location and (b) order of multiplexing as claimed in claims 8 and 18. Rather, *Robinett, et al.* only discloses a control circuit which obtains control of descriptor and transport packet storage locations.

Dobson, et al. appears to disclose a FIFO buffer 32 which signals a MUX microprocessor 22 when sufficient video data is in a buffer 32 (column 3, line 65-column 4, line 3).

Thus, *Dobson, et al.* only discloses signaling when sufficient video data is in a buffer. Nothing in *Dobson, et al.* shows, teaches or suggests (a) calculating an order of multiplexing based on storage location and (b) generating multiplexing instruction data which describe the storage location and order of multiplexing as claimed in claims 8 and 18. Rather, *Dobson, et al.* only discloses signaling when a buffer contains sufficient video data.

Furthermore, *Dobson, et al.* merely discloses that a processor 22 is alerted when there is a video start-code in a transport packet payload that is about to be read (column 4, lines 11-13).

Thus, *Dobson, et al.* merely discloses alerting a processor when a start-code is about to be read. Nothing in *Dobson, et al.* shows, teaches or suggests (a) calculating an order of multiplexing based on storage location and (b) generating multiplexing instruction data which describe the storage location and order of multiplexing as claimed in claims 8 and 18. Rather, *Dobson, et al.* only discloses alerting a processor when a start-code is about to be read.

The combination of *Robinett, et al.* and *Dobson, et al.* would merely suggest having a control circuit obtain control of descriptor and transport packet storage locations as taught by *Robinett, et al.* and signaling when a buffer contains sufficient video data and when a start-code is about to be read as taught by *Dobson, et al.* Thus, nothing in the combination of the references shows, teaches or suggests (a) calculating an order of multiplexing based on storage location and (b) generating multiplexing instruction data which describe (both) the storage location and order of multiplexing as claimed in claims 8 and 18. Therefore, Applicant respectfully requests the Examiner withdraws the rejection to claims 8 and 18 under 35 U.S.C. § 103.

Claims 9 and 19 recite additional features. Applicant respectfully submits that claims 9 and 19 would not have been obvious within the meaning of 35 U.S.C. § 103 over *Robinett, et al.* and *Dobson, et al.* at least for the reasons as set forth above. Therefore, Applicant respectfully requests the Examiner withdraws the rejection to claims 9 and 19 under 35 U.S.C. § 103.

Claims 10 and 20 were rejected under 35 U.S.C. § 103 as being unpatentable over *Robinett, et al.* in view of *Zaun, et al.* (U.S. Publication No. 2001/0024456).

As discussed above, *Robinett, et al.* merely discloses obtaining control of descriptor and transport packet storage locations. Nothing in *Robinett, et al.* shows, teaches or suggests (a) calculating an order of multiplexing based on storage location and (b) generating a plurality of multiplexing instruction data which describe (both) the storage location and order of multiplexing as claimed in claims 10 and 20.

Zaun, et al. appears to disclose an output processor 124 which generates two or more output streams from data stored in packet buffers 104. The output processing section then generates two or more independent high-speed transport multiplex output streams incorporating the selected packet data [0035].

Thus, *Zaun, et al.* merely discloses outputting two or more streams. Nothing in *Zaun, et al.* shows, teaches or suggests (a) calculating an order of multiplexing based on storage location and (b) generating multiplexing instruction data which describe (both) the storage location and order of multiplexing as claimed in claims 10 and 20. Rather, *Zaun, et al.* only discloses creating two or more output streams.

The combination of *Robinett, et al.* and *Zaun, et al.* would merely suggest to obtain control of descriptor and transport packet storage locations as taught by *Robinett, et al.* and to generate two or more output streams as taught by *Zaun, et al.* Thus, nothing in the combination

of the references shows, teaches or suggest (a) calculating an order of multiplexing based on storage location and (b) generating multiplexing instruction data which describe the storage location and order of multiplexing as claimed in claims 10 and 20. Therefore, Applicant respectfully requests the Examiner withdraws the rejection to claims 10 and 20 under 35 U.S.C. § 103.

New claims 21-5- have been added. Applicant respectfully points out that these claims have been allowed in the corresponding EP application.

Thus, it now appears that the application is in condition for a reconsideration and allowance. Reconsideration and allowance at an early data are respectfully requested.

CONCLUSION

If for any reason the Examiner feels that the application is not now in condition for allowance, the Examiner is requested to contact, by telephone, the Applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed within the currently set shortened statutory period, Applicant respectfully petitions for an appropriate extension of time. The fees for such extension of time may be charged to Deposit Account No. 50-0320.

In the event that any additional fees are due with this paper, please charge to our Deposit Account No. 50-0320.

Respectfully submitted,

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